AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of using a vector network analyzer (VNA) for coordinated Voltage Standing-Wave Ratio (VSWR) and Time Domain Reflectometry (TDR) measurement, said method comprising:

configuring said VNA for identifying discontinuities correlated to a VSWR lobe.

2. (Original) The method of claim 1 additionally comprising:

identifying a largest VSWR lobe in the frequency band of interest;

using phase data associated with S_{11} scattering parameter to find the correct electrical delay required to align Low Pass Step Transform data; and

configuring said Low Pass Step Transform span and center time to align coherent inductive and capacitive discontinuities relative to grid lines of a TDR display.

3. (Original) The method of claim 2 additionally comprising:

setting a first channel to Low Pass Step Transform and a second channel to a scattering parameter S_{11};

finding f_0, the frequency at the peak amplitude of the largest lobe of said scattering parameter S_{11} in the frequency band of interest;

setting electrical delay to zero;

finding the phase of S_{11} at f_0;

denoting said phase θ (degrees);

setting electrical delay in said first and said second channels to $(90-\theta)/(360 * f_0)$, such that said S_{11} lobe phase reads 90 degrees;

setting said first channel span to $10/ f_0$;

setting said first channel center to 0.4*span; and

setting said first channel format to real.

4. (Original) The method of claim 3 additionally comprising:

ensuring a valid 1-port calibration is performed on said VNA;

setting said first channel reference position to five divisions;

setting said first channel reference value to zero; and

setting said first channel scale to 0.05 units per division.

5. (Original) The method of claim 2 additionally comprising repeating said method for any additional problem VSWR lobes in said frequency band of interest, in order of decreasing lobe magnitude.

6. (Original) The method of claim 2 further comprising calibrating the magnitudes of capacitive, inductive, and resistive discontinuities, thereby allowing the design of correctly sized compensating features.

7. (Original) The method of claim 3 wherein said method is performed manually.

8. (Original) The method of claim 3 wherein said method is performed automatically.

9. (Original) The method of claim 8 additionally comprising:

providing a suitable VNA;

placing by a user a user-scrollable display marker on a VSWR or S_{11} lobe of interest;

pressing a control key by said user, thereby initiating automated execution of said method; and

automatically displaying a Low Pass Step Transform with correct time alignment for identifying coherent, canceling, and orthogonal circuit discontinuities.

10. (Original) The method of claim 9 wherein said suitable VNA comprises:

a visual display;

a processor operable to process time domain and frequency domain reflection signals for graphic presentation on said visual display, said processor capable of performing VNA state control and vector mathematical operations: and

wherein said display includes a visual display marker having a recognizable shape.

11. (Original) The method of claim 6, wherein said method is performed automatically.

12. (Original) The method of claim 11 additionally comprising:

providing a suitable VNA; and

calculating the relationship of discontinuity amplitude to excess capacitance and/or excess inductance using a processor associated with said VNA.

13. (Original) The method of claim 12 additionally comprising placing a user-scrollable display marker on a time-domain discontinuity;

14. (Original) The method of claim 12 additionally comprising accepting at a user interface of said VNA y-axis scaling unit inputs of pF per division and/or nH per division.

15. (Original) The method of claim 12 additionally comprising selecting via a calibration enunciator of a TDR display of said VNA a scale in pF per division and/or nH per division in response to user interface entry of units per division.

16-21. (Canceled)